Morse Micro

reaching farther™

MM6108

IEEE 802.11ah Sub-1 GHz 1/2/4/8 MHz Bandwidth MAC/PHY/Radio SoC

Advanced Data Sheet

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1. Product Overview

1.1. Introduction

Morse Micro provides a complete Wi-Fi HaLow connectivity solution. The MM6108 SoC is a single-chip solution, including Radio, PHY, and MAC sections designed in compliance with the IEEE 802.11ah standard, supporting data rates up to 32.5 Mbps. The standard provides for operation in the sub-1 GHz license exempt RF bands[1]. The Radio in the MM6108 supports programmable operation in these bands, worldwide, between 850 MHz and 950 MHz.

The MM6108 has been designed for a simplified Wi-Fi HaLow connection to an external host for applications in which a customer wants to replace their prior RF technology with a Wi-Fi HaLow connection.

The RF interface for the MM6108 includes the option to use either the on-chip amplification for typical low-power, low-cost devices, or in conjunction with an external PCB mount power amplifier for Ultra-Long-Reach applications.

The RF receiver features a high linearity LNA, making the use of external filters unnecessary in many applications.

Security features required for Wi-Fi HaLow product certifications are supported by MM6108.

Battery-operated applications are supported by a combination of features in the MM6108. The IEEE 802.11ah standard provides for extended sleep times of battery-operated Stations (STAs or client devices), with longer durations than other prior IEEE 802.11a/b/g/n/ac generations. It also allows longer extended maximum idle times for clients to conserve energy without being removed from the access point's (AP's) list of authenticated devices.

[1] These are typically the unlicensed Industrial Science and Medical (ISM) bands in ITU Region 2 (USA, Canada, South America etc) and are also available in other countries usually with class license requirements.

1.2. Features

Single Chip Wi-Fi HaLow Transceiver for Low-Power, Long-Reach IoT Applications:

- Single-stream max data rate of 32.5 Mbps (MCS=7, 64-QAM, 8 MHz channel, 4µs GI)
- Radio supporting worldwide Sub-1 GHz frequency bands
    - Frequency range: 850-950 MHz
    - Channel bandwidth options of 1/2/4/8 MHz
    - Max output power: 8 dBm
- 802.11ah OFDM PHY
    - BPSK & QPSK, 16-QAM & 64-QAM Modulation
    - Automatic frequency & gain control
    - Packet detect & channel equalization
    - Forward Error Correction (FEC) coding & decoding
    - Supports Modulation and Coding Scheme (MCS) levels MCS 0-7 and MCS 10
    - Supports 1 MHz duplicate mode
    - Supports optional Traveling Pilots and Short Guard Intervals
- 802.11ah MAC supporting WFA HaLow certification
    - Support for STA and AP roles
    - Listen-Before-Talk (LBT) access with energy detect
    - 802.11 power save
    - 802.11 fragmentation and defragmentation
    - Packet aggregation
    - Power-Saving Target Wake Time (TWT) support for long battery life
    - Restricted Access Window (RAW)
    - Automatic and manual MCS rate selection
- SDIO 2.0 compliant slave interface
    - SDIO 2.0 Default Speed (DS) at 25 MHz
    - SDIO 2.0 High Speed (HS) at 50 MHz
    - Support for both 1-bit and 4-bit data mode
    - Support for SPI mode operation
- Power Management Unit (PMU) for various modes of operation
    - Power-down (interrupt driven wake)
    - Hibernate mode (internal / external wake)
    - Active Receive / Transmit mode
    - Integrated DC-DC converter supporting a voltage supply from 3.0V to 3.6V
- RF Interface
    - On-chip 8dBm output power, with option to use external PA or FEM
    - Option to use an external LNA or FEM
- Wide spectrum of security features
    - AES encryption engine
    - Hardware support for SHA1 and SHA2 hash functions (SHA-256, SHA-384, SHA-512)
    - WPA3 including protected management frames (PMF)
    - Opportunistic Wireless Encryption (OWE)

1.3. Applications

For Internet of Things (IoT) and Machine-to-Machine (M2M) applications such as:

- Surveillance Cameras and Sensors
- Cloud Connectivity
- Low-power Sensor Networks
- Building Automation Systems (BAS)
- Asset Tracking and Management
- Machine Performance Monitors & Sensors
- Building Access Control & Security
- Drone Video and Navigation Communications
- Connected Toys and Games
- Rural Internet Access
- Agricultural and Farm Networks
- Utility Smart Meter and Intelligent Grid
- Proximity Sensors
- Industrial Automation Controls
- Smart Home Automation
- EV Car Chargers
- Appliances
- Construction Site Connectivity
- Smart Signs and Kiosks
- Retail Point-of-Sale Terminals
- Vehicle-to-Vehicle or Vehicle-to-Infrastructure Communications
- IP Sensor Networks
- Biometric IDs and Keypads
- Warehouse Connectivity
- Intelligent Lighting Controls
- BT/ZigBee(™)/Z-Wave(™) to Wi-Fi HaLow Gateways
- Wi-Fi to Wi-Fi HaLow Bridges
- Wi-Fi HaLow Client Adapters/Dongles
- Smart City Networks

2. Pin Descriptions

The MM6108 device has 48-pins, which are described in this section. The following illustration shows the top view of the MM6108 pin Diagram.

Figure 1: Pin Diagram

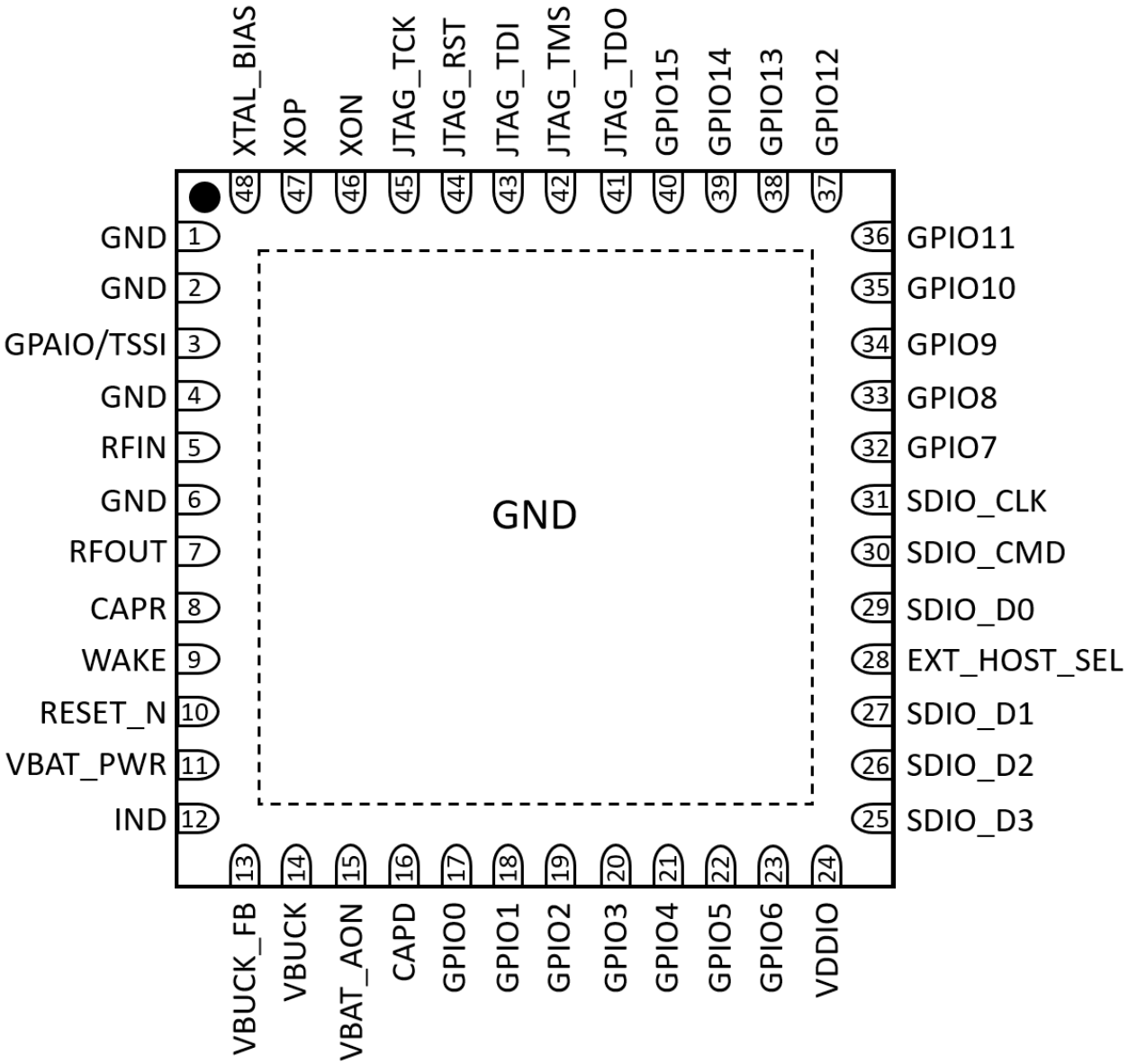


Table 2: Pin Description

Pin	Pin Name	Type	Description
1	GND	Ground	Ground
2	GND	Ground	Ground
3	GPAIO/TSSI	Analog	Optional Transmit signal strength Indication from FEM
4	GND	Ground	Ground
5	RFIN	RF	RF input
6	GND	Ground	Ground
7	RFOUT	RF	RF output
8	CAPR	Power	Bypass capacitor connection for RF supply
9	WAKE[4]	Input	WAKE from sleep input
10	RESET_N[4]	Input	Asynchronous chip reset (active low)
11	VBAT_PWR	Power	IC Power Supply
12	IND	Analog	Inductor connection for integrated power management
13	VBUCK_FB	Power	Connection for integrated power management
14	VBUCK	Power	Connection for integrated power management
15	VBAT_AON	Power	IC Power Supply (VBAT_AON and VBAT_PWR must be connected to the same source)
16	CAPD	Power	Bypass capacitor connection for digital supply
17	BUSY[5]	Digital I/O	Wi-Fi Busy
18	GPIO1[5]	Digital I/O	GPIO
19	GPIO2[5]	Digital I/O	GPIO
20	GPIO3[5]	Digital I/O	GPIO
21	GPIO4[5]	Digital I/O	GPIO
22	GPIO5[5]	Digital I/O	GPIO
23	GPIO6[5]	Digital I/O	GPIO
24	VDDIO	Power	VDD supply for digital IO
25	SDIO_D3[3][5]	Digital I/O	SDIO Data 3
26	SDIO_D2[3][5]	Digital I/O	SDIO Data 2
27	SDIO_D1[3][5]	Digital I/O	SDIO Data 1
28	EXT_HOST_SEL[5]	Digital I/O	External Host Select
29	SDIO_D0[3][5]	Digital I/O	SDIO Data 0
30	SDIO_CMD[3][5]	Digital I/O	SDIO Command
31	SDIO_CLK[5]	Digital I/O	SDIO Clock
32	GPIO7[2][5]	Digital I/O	GPIO
33	GPIO8[2][5]	Digital I/O	GPIO
34	GPIO9[2][5]	Digital I/O	GPIO
35	GPIO10[2][5]	Digital I/O	GPIO
36	GPIO11[2][5]	Digital I/O	GPIO/ RF FEM CTRL
37	GPIO12[2][5]	Digital I/O	GPIO/ RF FEM CTRL
38	GPIO13[2][5]	Digital I/O	GPIO/ RF FEM CTRL
39	GPIO14[2][5]	Digital I/O	GPIO/ RF FEM CTRL
40	GPIO15[2][5]	Digital I/O	GPIO/ RF FEM CTRL
41	JTAG_TDO[1]	Digital I/O	JTAG Data Out
42	JTAG_TMS[1]	Digital I/O	JTAG Mode Select
43	JTAG_TDI[1]	Digital I/O	JTAG Data In
44	JTAG_TRST[1]	Digital I/O	JTAG Reset
Pin	**Pin Name**	**Type**	**Description**

45	JTAG_TCK[1]	Digital I/O	JTAG Clock
46	XON	Analog	32 MHz crystal component connection
47	XOP	Analog	32 MHz crystal component connection
48	XTAL_BIAS	Analog	Crystal Bias
-	GND	Ground	Exposed ground pad - must connect to PCB ground

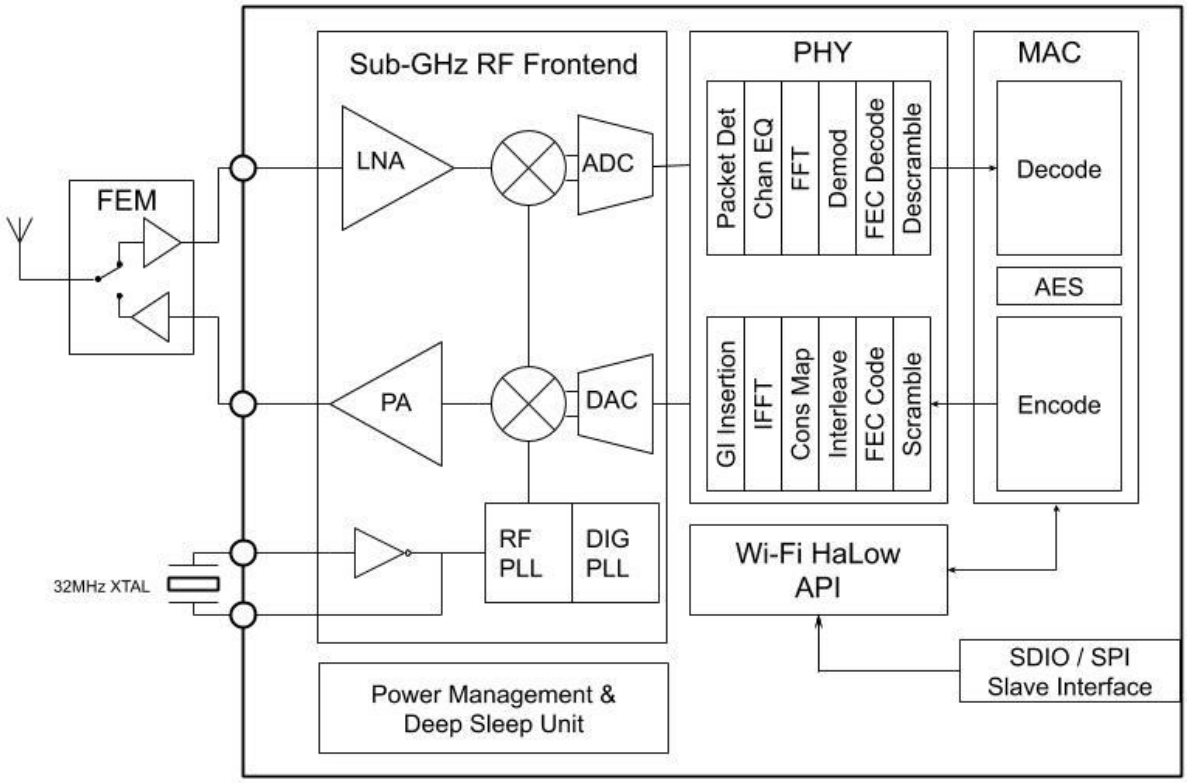
[1] JTAG pins should be tied to GND via a 10k pull down resistor
[2] All unused GPIO should be tied to GND via a 10k pull down resistor
[3] All SDIO bus pins should be pull up with a 10k-100k resistor as per the the SDIO standard
[4] Supplied from VBAT domain. Other pins driven by VDDIO domain.
[5] See Section 4.1 for the GPIO Alternate functions

3. Functional Description

The following sections describe the functions of the MM6108 SoC.

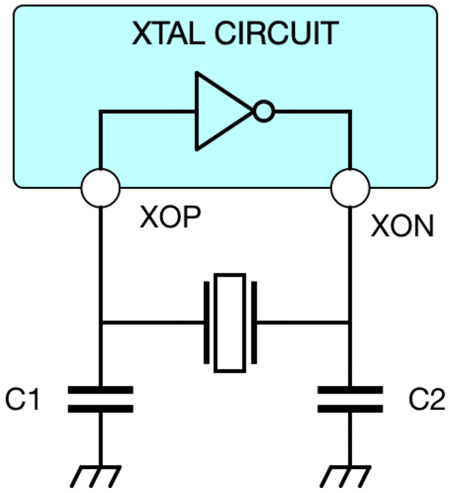
3.1. Functional Block Diagram

Figure 1: Functional Block Diagram



3.2. Clocks

The MM6108 uses a 32 MHz crystal component to derive all clocks used in the system. A Pierce oscillator circuit is used as shown in figure:



The crystal should be connected between pins XOP & XON. Load capacitors C1 and C2 should be high accuracy NP0 dielectric. The total capacitance on XOP and XON nodes should be twice that of the load capacitance specified by the crystal component (CL):

C1 = C2 = 2 x CL

To adhere to 802.11ah standards for frequency offset and achieve specified sensitivity the crystal component should adhere to the following specifications:

Table 2: RF Crystal Specification

Parameter	Min	Max	Units
Frequency tolerance	-20	+20	ppm
ESR	10	50	ohms

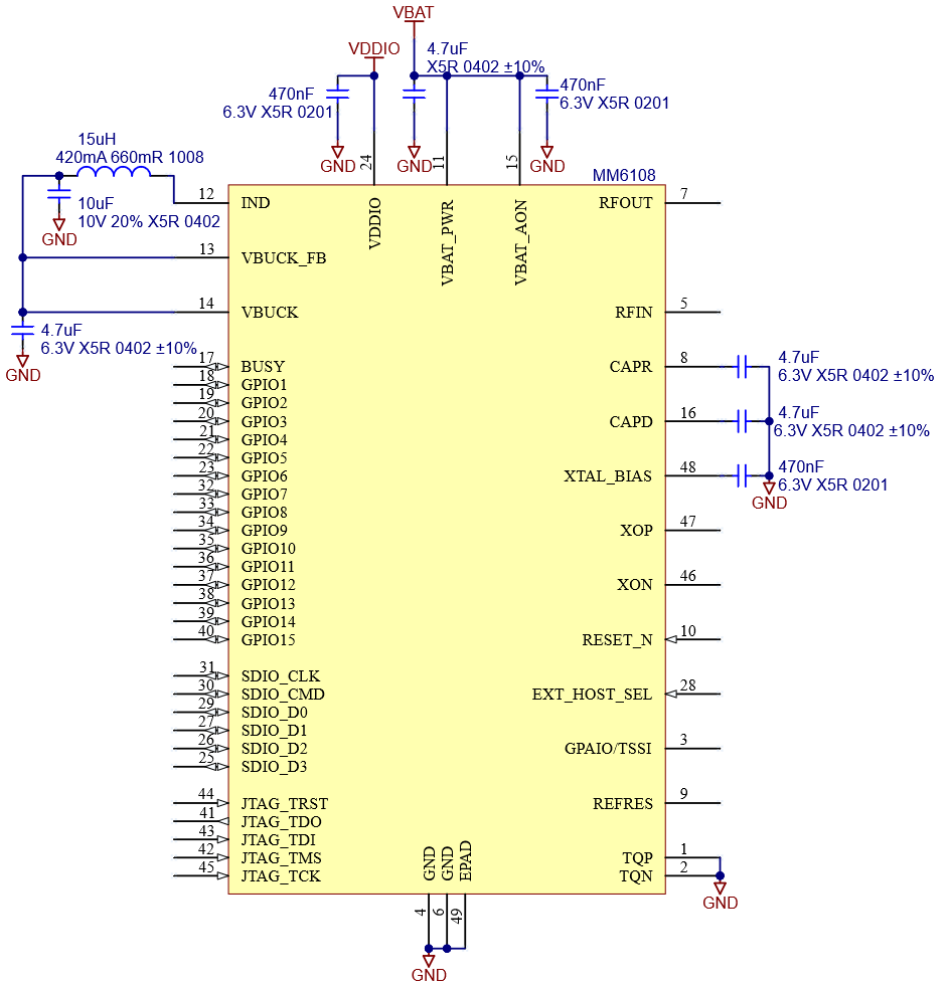
3.3. Power Management

All power is derived from a single 3.0V to 3.6V supply provided on pin VBAT_PWR and VBAT_AON. There is an internal buck converter, which requires a 15uH inductor between pins IND and VBUCK_FB, and a 10uF ceramic capacitor in VBUCK.

There are three internal power supplies: RF, Analog, and Digital. These are regulated by internal circuits and required decoupling capacitors on the PCB: CAPR, CAPD, and VBAT_AON should be 4.7uF ceramic capacitors.

To avoid damage to the device, ensure that VDDIO does not exceed VBAT.

For normal boot operation, ensure that the JTAG_TRST pin is held in reset by pulling to ground with a 10kOhm resistor.



Note: VDDIO supplies the digital input and output pads

4. Digital Interfaces

4.1. Pin Allocation

The chip's digital pins are allocated as per the following table. Multiple-function pins are indicated.

Pin	Name	Default function	IO Function 0	IO Function 1	Further function
17	BUSY	BUSY	PWM1 bit 0	SPI0 CS3	GPIO0
18	GPIO1	GPIO	PWM1 bit 1		1 wire EEPROM
19	GPIO2	GPIO	UART0 Rx	PWM1 bit 2	
20	GPIO3	GPIO	UART0 Tx	PWM1 bit 3	
21	GPIO4	GPIO	I^2C SDA		
22	GPIO5	GPIO	I^2C SCL		
23	GPIO6	GPIO	UART1 Rx		
25	SDIO_D3	Data pin 3	Unused	Chip select	HOLD (IO_3)
26	SDIO_D2	Data pin 2	Unused	Unused	WP (IO_2)
27	SDIO_D1	Data pin 1	IRQ	IRQ	DO (IO_1)
28	EXT_HOST_SEL	SDIO/SPI device strap (tie high)			SPI master strap (tie low)
29	SDIO_D0	Data pin 0		MISO	DI (IO_0)
30	SDIO_CMD	Command pin		MOSI	Chip select
31	SDIO_CLK	Clock (input)			Clock (Output)
32	GPIO7	GPIO	UART1 Tx		
33	GPIO8	GPIO	SPI0 SCK		
34	GPIO9	GPIO	SPI0 CS0		
35	GPIO10	GPIO	SPI0 D0		
36	GPIO11	GPIO	SPI0 D1		
37	GPIO12	GPIO	PWM0 bit 0	SPI0 CS1	FEM Control
38	GPIO13	GPIO	PWM0 bit 1	SPI0 D2	FEM Control
39	GPIO14	GPIO	PWM0 bit 2	SPI0 D3	FEM Control
40	GPIO15	GPIO	PWM0 bit 3	SPI0 CS2	FEM Control

4.1.1. GPIO function selection

The 16 GPIO pins support multiple different hardware functions as specified in the table above. Each pin may be individually configured to select one of the up-to 4 controlling hardware functions.

4.1.2. SDIO/SPI function selection

Pins 30, 29, 27, 26, 25 (the SDIO/SPI interface) are configured via the strap pin EXT_HOST_SEL. Strap the pin high (1) to expose the SDIO/SPI device interface. Strap the pin low (0) to expose the SPI flash master interface.

4.2. SDIO Device

A host interface via SDIO 2.0 at either default or high speed, operating at 3.3V, is available.
To expose the SDIO interface pins, pin 28 EXT_HOST_SEL must be pulled up to VDDIO, indicating the presence of an external host.

4.2.1. Pins

Pin	Name	SDIO 4-bit mode	SDIO 1-bit mode
25	SDIO_D3	Data pin 3	Unused
26	SDIO_D2	Data pin 2	Unused
27	SDIO_D1	Data pin 1	IRQ
28	EXT_HOST_SEL	SDIO/SPI/QSPI interface enable strap (tie high)	
29	SDIO_D0	Data pin 0	
30	SDIO_CMD	Command pin	
31	SDIO_CLK	Clock pin (input)	

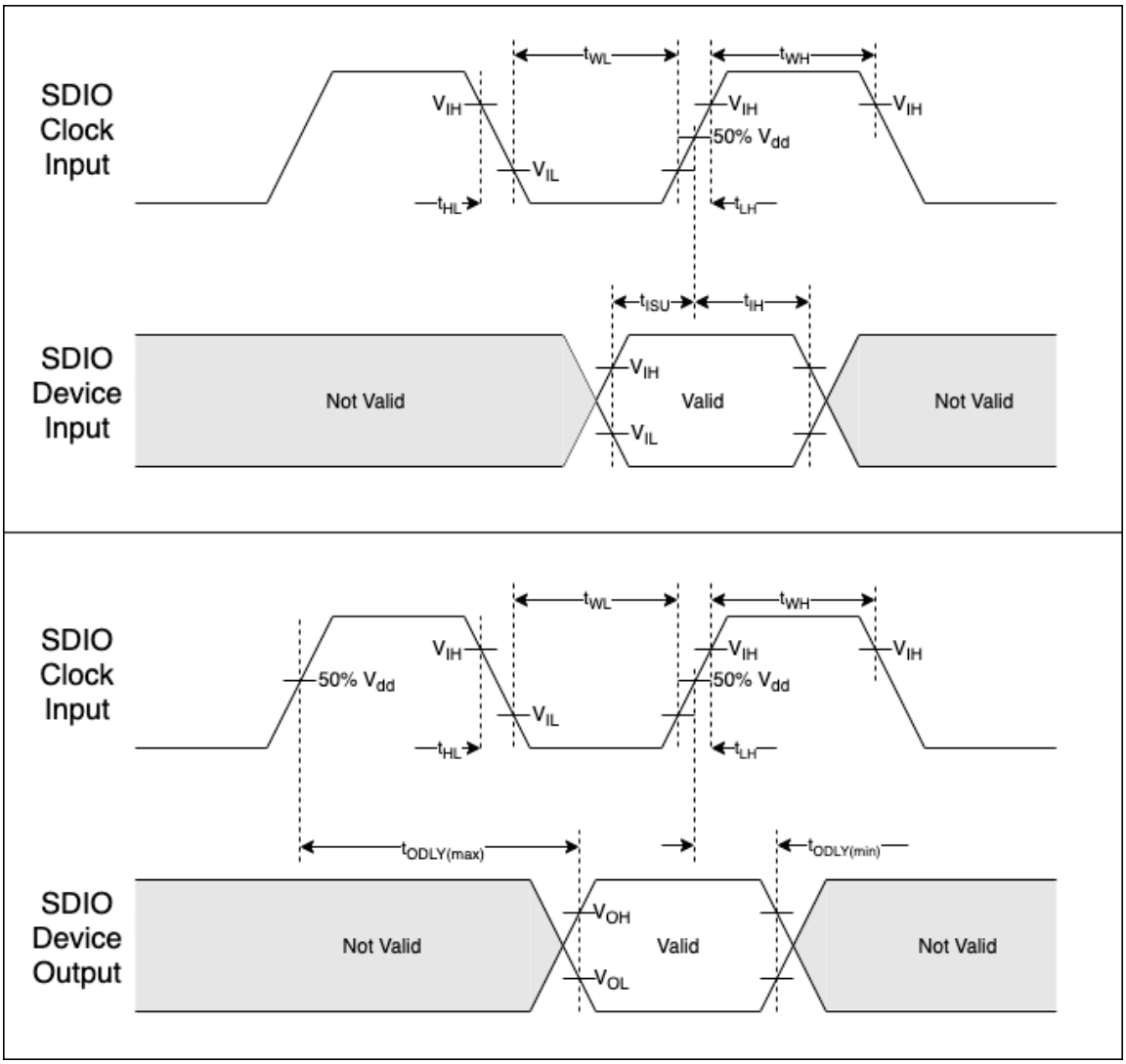
Note: Unused pins should be pulled high.

4.2.2. Functions

Internally the SDIO will present two functions (in addition to the mandatory function 0) to be used to access the chip. Functions 1 and 2 only differ in the maximum transfer size they support. Function 1 can perform transactions up to 8 bytes at a time, function 2 supports up to 512 bytes at a time, making it better suited to bulk data transfers.

4.2.3. Bus Timing

The SDIO interface supports a clock rate up to 50 MHz.



Parameter	Min	Max
Clock parameters		
Clock frequency	0 MHz	50 MHz
Clock low time (t_{WL})	7ns	
Clock high time(t_{WH})	7ns	
Clock rise time (t_{LH})		3ns
Clock fall time (t_{HL})		3ns
Inputs on CMD, DAT lines to device from host		
Input setup time (t_{ISU})	6ns	
Input hold time (t_{IH})	2ns	
Outputs on CMD, DAT lines from device to host		
Output delay ($t_{ODLY(max)}$)		14ns
Output hold time ($t_{ODLY(min)}$)	2.5ns	
Total system capacitance for each line		40pF

4.3. SPI Device

The SPI interface uses the physical unidirectional pin layout as defined below, over which the modified SDIO protocol is used for communication.

4.3.1. Pins

Pin	Name	SPI mode function
25	CS	Chip select (active low)
26	NC	Not connected/unused (tie to VDDIO)
27	INT	Interrupt pin
28	EXT_HOST_SEL	SDIO/SPI/QSPI interface enable strap (tie to VDDIO)
29	MISO	Master data in/slave data out
30	MOSI	Master data out/slave data in
31	CLK	Clock pin (input)

4.3.2. Initialization in SPI mode

After power-on, the host interface can be either SDIO or SPI. To put the interface to SPI mode, the host must send a CMD0 while holding CS low (asserted).

For further details on the protocol, see the SD Specification Part E1 “SDIO Simplified Specification” version 2.00.

4.3.3. SPI Bus Timing

The SPI clock rate supports up to 50 MHz. The SPI bus timing is identical to the SDIO bus timing, where MOSI and MISO are considered input and output timing, respectively, in the SDIO timing specification.
The SPI bus defaults to clock idling at logical 0 (CPOL=0), and data is launched and captured on the positive edges of the clock, as per SDIO high-speed mode. It may be configured to behave like CPHA=0 (drive output on negative edge, sample on positive edge) after being initialized.

4.4. GPIO

There are 16 GPIO pins. Each pin can be controlled as a standard GPIO and is overloaded with hardware peripherals, as detailed in the digital pin section.

4.4.1. Features

When assigned to GPIO control, the pin's pad controls are directly connected to the GPIO hardware. This hardware consists of a register to set each pin's drive enable, drive value and read the value present on the pin (whether driving or not).
Each pin can also be configured to generate an interrupt based on level, or edge (rising or falling). Each pin can be an individual interrupt source via the platform interrupt controller. Inputs are synchronized to the main digital clock and so any pulses must be at least a few cycles of this clock to be detectable.
There are no internal pull-up or pull-down facilities in the pads, nor drive-strength selection.

4.4.2. Reset state

At reset every GPIO pin will be undriven and in a high-impedance state.

4.4.3. Power-save state

During power-save the digital GPIOs will go high-impedance. These pins should be pulled up/down or driven to ensure the lowest sleep currents can be achieved.

4.4.4. Configuration

The default state of each of these pins is to be a software-controlled GPIO. The per-pin IO Function Enable register, which selects whether GPIO or other hardware controls the pin, will need to be cleared for the GPIO hardware to own the pin.

4.5. SPI Master

SPI master supports operation over the single-lane, dual-lane and quad-lane. This is used for accessing SPI slaves (up to 4 slaves, one active at a time).

4.5.1. Pins

The pins are mapped as shown in the following table:

Pin	Name	Default function	IO Function 0	IO Function 1
17	GPIO0	GPIO		SPI0 CS3
33	GPIO8	GPIO	SPI0 SCK	
34	GPIO9	GPIO	SPI0 CS0	
35	GPIO10	GPIO	SPI0 D0	
36	GPIO11	GPIO	SPI0 D1	
37	GPIO12	GPIO		SPI0 CS1
38	GPIO13	GPIO		SPI0 D2
39	GPIO14	GPIO		SPI0 D3
40	GPIO15	GPIO		SPI0 CS2

4.5.2. Bus Timing

The bus timing specification is the same as per section 4.2.3.

4.6. I²C Master

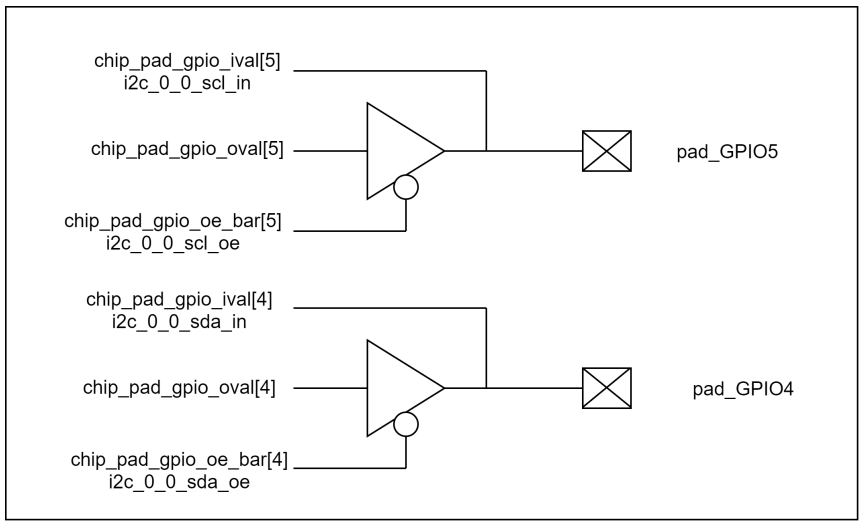
An I²C master interface is available. It consists of two lines, SDA and SCL, which are bidirectional, connected to a positive supply voltage via a current-source or pull-up resistor.

4.6.1. Pin Description

As mentioned in section 4.1, Pin 21 - GPIO4 and Pin 22 - GPIO5 are used as I²C SDA and I²C SCL respectively.

Pin	Name	Default function	IO Function 0
21	GPIO4	GPIO	I²C SDA
22	GPIO5	GPIO	I²C SCL

Connections would be made according to the following figure:



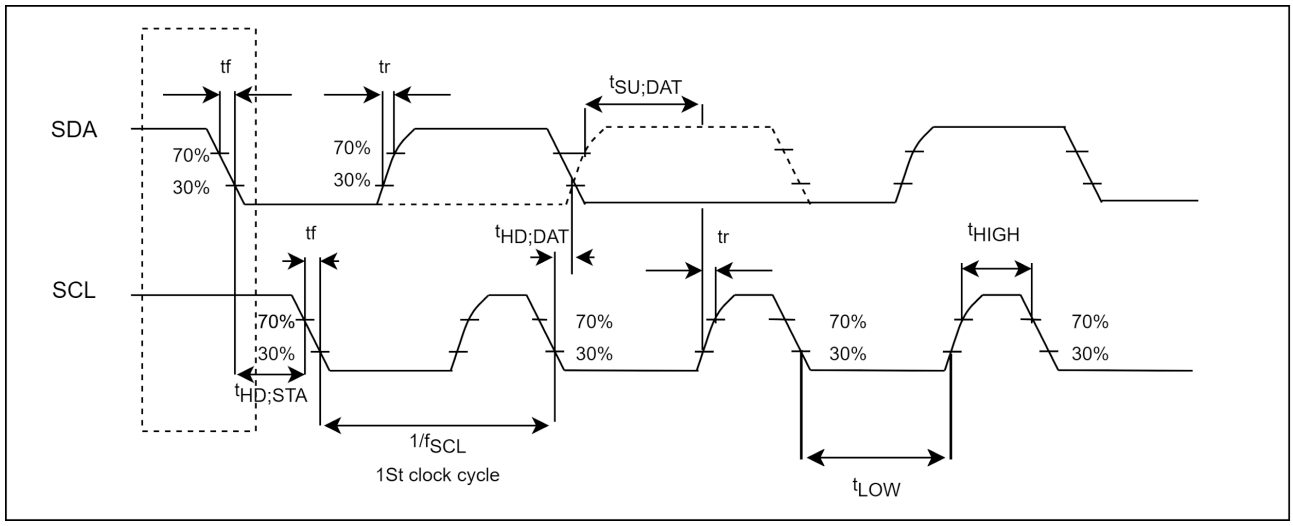
4.6.2. Bus Speed

The I²Cmaster is 8-bit oriented and bidirectional. The data transfers can be made at the following speeds:

- Standard-mode (Sm), with a bit rate up to 100 kbit/s
- Fast-mode (Fm), with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+), with a bit rate up to 1 Mbit/s
- High-speed mode (Hs-mode),with a bit rate up to 3.4M/bits

4.6.3. Bus Timing

Fig. Definition of timing for F/S-mode devices on the I²C-bus. All values referred to $V_{IH(min)}$(0.3V_{DD}) and $V_{IL(max)}$(0.7V_{DD})levels.



Parameter	Standard-mode		Fast-mode	
	Min	Max	Min	Max
Clock frequency(f_{SCL})	0	100kHz	0	400kHz
Fall time of both SDA and SCL (t_f)	-	300ns	20x (V_{DD}/5.5V)	300ns
Rise time of both SDA and SCL signals(t_r)	-	1000ns	20ns	300ns
Data hold time ($t_{HD;DAT}$)	5.0us	-	-	-
Data set-up time ($t_{SU;DAT}$)	250ns	-	100ns	-
LOW period of the SCL clock	4.7us	-	1.3us	-
HIGH period of the SCL clock	4.0us	-	0.6us	-
Hold time- START,first clock is generated after this($t_{HD;STA}$)	4us	-	0.6us	-

4.7. UART

Two universal asynchronous receiver/transmitter (UARTs) are available and provide a means for serial communication to off-chip devices. The UART peripheral does not support hardware flow control or other modem control signals, or synchronous serial data transfers.

4.7.1. Features

The UART peripheral supports the following features:

- 8-N-1 and 8-N-2 formats: 8 data bits, no parity bit, 1 start bit, 1 or 2 stop bits
- 8-entry transmit and receive FIFO buffers with programmable watermark interrupts
- 16× Rx oversampling with 2/3 majority voting per bit

4.7.2. Pin Description

Pin	Name	Default function	IO Function 0
19	GPIO2	GPIO	UART0 Rx
20	GPIO3	GPIO	UART0 Tx
23	GPIO6	GPIO	UART1 Rx
32	GPIO7	GPIO	UART1 Tx

4.8. JTAG

A JTAG interface is provided for chip debug and test purposes. Its circuitry will not be reset by anything other than the reset from the JTAG interface pin. [Ensure pin 44 (JTAG_RST) is tied to the ground during chip boot.] This may cause problems when the chip is power-cycled whilst JTAG is not in reset.

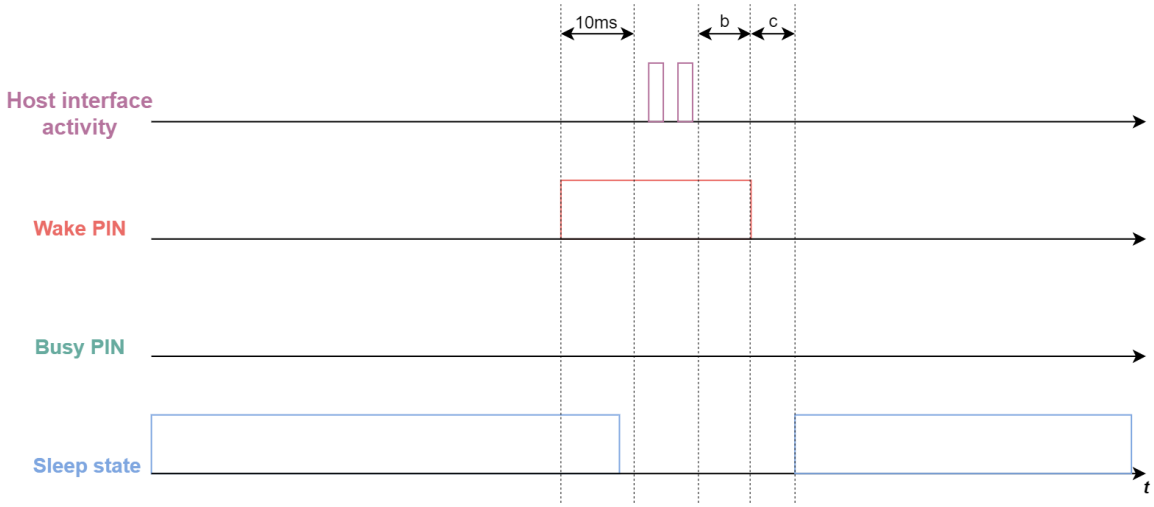
Functionally the JTAG will be the standards-compliant protocol interface and provide access to:

- custom internal test logic enables (scan mode, MBIST mode)
- SiFive RISC-V debug logic for CPU and system debug
- Morse Micro custom JTAG overrides “Get-out-of-Jail” (GooJ) block registers

The JTAG interface will be constrained to 50 MHz in mission/functional and scan modes.

4.9. Sleep/Wake Sequencing

4.9.1. Host wakes MM6108 from sleep

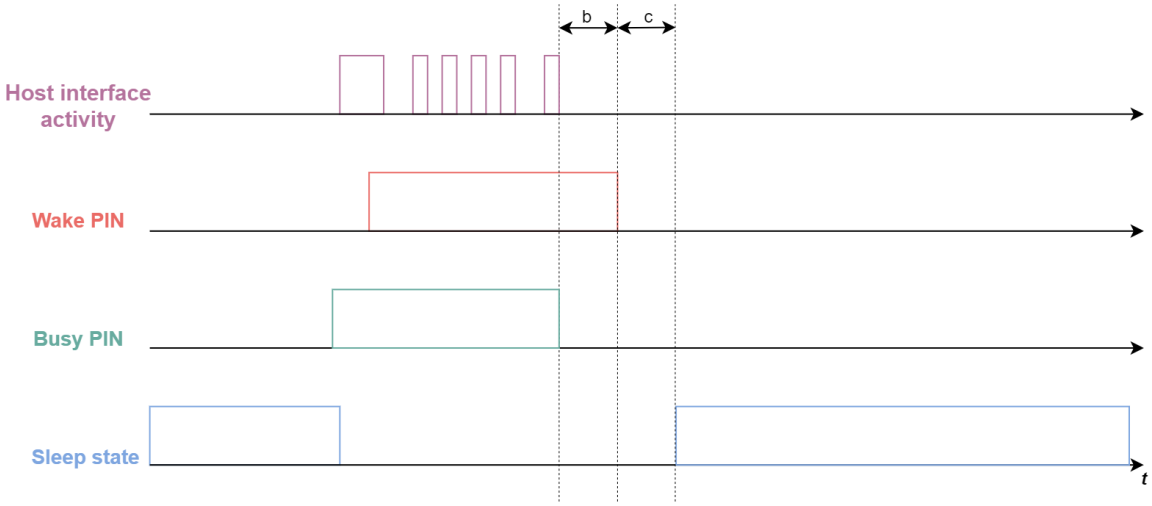


1. The driver will raise the wake pin and wait a static period, before initializing the shared communication bus and initiating host interface activity. On MM6108, this period is typically 10ms.

2. After completing communication the driver will wait a static period, **b**, before lowering the wake pin (assuming no further communication has occurred). Depending on the nature of the communication (802.11 data vs. commands) this period can range from 5 to 90ms.

3. After the wake pin has fallen, the MM6108 will wait a period, **c**, before initiating hardware sleep. This period is dynamic and will differ depending on the power-save protocol in use and other chip-specific factors

4.9.2. MM6108 wakes host from sleep (with host interface disabled)



1. The MM6108 wakes from sleep and realizes it needs to pass traffic or an event to the host. It begins by asserting the busy pin.

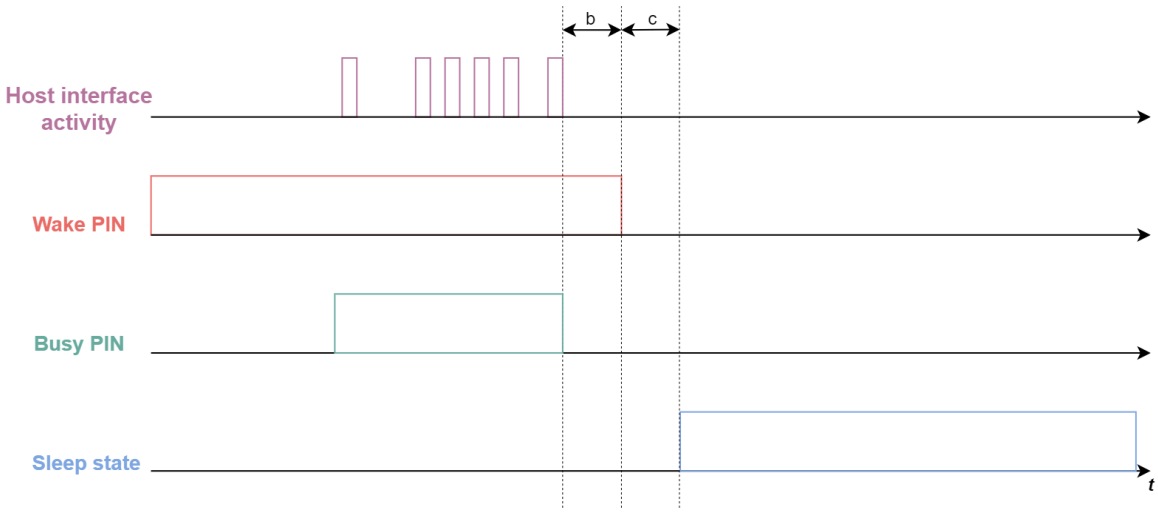
2. The busy pin will fire an interrupt on the host, after which the host will immediately
    a. Raise the Wake PIN.
    b. Wait a static period, 10ms
    c. Initializes / enables the shared host interface.

3. After asserting the busy pin, the MM6108 will immediately begin initiating host interface communication. It does not wait until the host 'enables' the shared host interface. This is okay, as the bus transaction will be waiting for the host and an interrupt should fire as soon as the host enables bus interrupts.

4. Once the MM6108 no longer needs to converse with the host, the busy pin will drop immediately. The host will wait a static period, **b**, before dropping the wake pin.

5. After the wake pin has fallen, the MM6108 will wait a period, **c**, before initiating hardware sleep.

4.9.3. MM6108 initiates communication with host (host interface enabled)



1. The MM6108 was previously woken by the host for communication.

2. Sometime after wake and host->MM6108 communication, the MM6108 realizes it needs to send data back to the host (MM6108->host). It will assert the busy pin.

3. The busy pin will fire an interrupt on the host, after which it will immediately

    a. Process the interrupt but perform no further action as the wake pin was already asserted and the shared host interface is currently enabled/initialized.

4. After MM6108->host communication completion, hardware sleep will be initiated as described above.

5. Electrical Characteristics

5.1. Absolute Max ratings

Stress beyond absolute maximum ratings may cause permanent damage to the device. Functional operation is guaranteed for recommended operation conditions only. Operation of the device outside of recommended conditions may result in reduced lifetime and/or reliability problems even if the absolute maximum ratings are not exceeded.

Parameter	Min	Max	Unit
VBAT voltage	-0.3	4.3	V
Voltage on digital I/O pin	-0.3	4.3	V
Voltage on analog/RF pin	-0.3	1.32	V
Storage Temperature	-40	125	°C
RF Input Power (CW)	-	6	dBm

5.2. Immunity

Parameter			Min	Max	Unit
Electrostatic discharge (ESD) performance	Human body model (HBM), per ANSI / ESDA / JEDEC JS001	RF Input	-500	500	V
		All pins except RF Input	-2000	2000	V
	Charged device model (CDM), per JESD22-C101	All pins	-500	500	V

5.3. Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Ambient Temperature (MM6108CQ)	-10	25	70	°C
Ambient Temperature (MM6108IQ)	-40	25	85	°C
V_{BAT} / V_{BAT_AON} [2]	3.0	3.3	3.6	V
VDDIO[1]	1.62	3.3	3.6	V
Digital I/O voltage	0	3.3	VDDIO	V

[1] VDDIO should not exceed VBAT

[2] V_{BAT_AON} should be greater than or equal to VBAT during power up.

Performance specifications are achieved under typical operating conditions, unless otherwise specified.

5.4. Power Consumption

5.4.1. Transmit power consumption

Mode	Condition T_A=25°C, V_{BAT}/V_{DDIO} = 3.3V	V_{BAT} Current			Unit
		Min	Typ	Max	
Transmit current (MCS7,3dBm, 100% D.C.)	1 MHz channel	33	43	53	mA
	2 MHz channel	39	45	52	mA
	4 MHz channel	46	52	60	mA
	8 MHz channel	56	63	76	mA
Transmit current (MCS0, 6dBm, 100% D.C.)	1 MHz channel	43	58	76	mA
	2 MHz channel	37	47	60	mA
	4 MHz channel	45	54	62	mA
	8 MHz channel	57	67	77	mA

5.4.2. Receive power consumption

Mode	Condition T_A=25°C, V_{BAT}/V_{DDIO} = 3.3V	V_{BAT} Current			Unit
		Min	Typ	Max	
Listen	1 MHz channel	22	26	31	mA
	2 MHz channel	24	28	33	mA
	4 MHz channel	27	32	38	mA
	8 MHz channel	32	37	43	mA
Active receive MCS7	1 MHz channel	24	26	35	mA
	2 MHz channel	28	30	39	mA
	4 MHz channel	34	40	46	mA
	8 MHz channel	45	53	61	mA
Active receive MCS0	1 MHz channel	20	26	35	mA
	2 MHz channel	26	28	36	mA
	4 MHz channel	30	36	46	mA
	8 MHz channel	45	48	59	mA

5.4.3. Sleep power consumption

Mode	Condition T_A=25℃, V_{BAT}/V_{DDIO} = 3.3V	V_{BAT}			Unit
		Min	Typ	Max	
Snooze	RC Oscillator on, Memory retained, configurable wake up timer	9.5	27	370	uA
Deep sleep	RC Oscillator on, configurable wake up timer	0.8	1	1.8	uA
Hibernate	Power off, wait for external interrupt	0.03	0.05	1	uA

5.4.4. DTIM3 power consumption

Mode	Condition T_A=25℃, V_{BAT}/V_{DDIO} = 3.3V, 102.4ms Beacon Interval	V_{BAT}			Unit
		Min	Typ	Max	
S1G beacons	1 MHz channel	370	385	395	uA
	2 MHz channel	370	385	395	uA
	4 MHz channel	265	275	285	uA
	8 MHz channel	265	275	285	uA
S1G beacons with proprietary DTIM signaling[2]	1 MHz channel	170	188	200	uA
	2 MHz channel	170	188	200	uA
	4 MHz channel	165	175	185	uA
	8 MHz channel	165	175	185	uA

5.4.5. DTIM10 power consumption

Mode	Condition T_A=25℃, V_{BAT}/V_{DDIO} = 3.3V, 102.4ms Beacon Interval	V_{BAT}			Unit
		Min	Typ	Max	
Legacy beacons	1 MHz channel	135	140	155	uA
	2 MHz channel	135	140	155	uA
	4 MHz channel	95	105	120	uA
	8 MHz channel	95	105	120	uA
S1G beacons with proprietary DTIM signaling[2]	1 MHz channel	80	85	100	uA
	2 MHz channel	80	85	100	uA
	4 MHz channel	75	80	95	uA
	8 MHz channel	75	80	95	uA

[2] Signaling that indicates whether a power save STA should receive and process an entire beacon

5.5. RF Specifications

5.5.1. Frequency Range

The MM6108 radio operates in the frequency range from 850 MHz to 950 MHz to cover the upper sub 1 GHz band.

Region	Sub 1 GHz bands available	Total BW available
USA	902 - 928 MHz	26 MHz
Europe	863 - 868 MHz 917.4 -919.4 MHz	7 MHz
Australia & New Zealand	915 - 928 MHz	13 MHz
Korea	917 - 923.5 MHz 925 - 931 MHz	12 MHz
Japan	915.9 - 928.1 MHz	11 MHz
Singapore	866 - 869 MHz 920 - 925 MHz	8 MHz
India	865 - 868 MHz	3 MHz

5.5.2. Receiver

5.5.2.1. Sensitivity

Sensitivities for 10% packet error rate, 1000 byte packets.

MCS index	Modulation scheme	Coding rate	Phy rate (kbps) per BW				Minimum Receive sensitivity (dBm) per BW			
			1 MHz	2 MHz	4 MHz	8 MHz	1 MHz	2 MHz	4 MHz	8 MHz
0	BPSK	1/2	333	722	1500	3250	-105	-103	-101	-97
1	QPSK	1/2	667	1444	3000	6500	-102	-100	-97	-93
2	QPSK	3/4	1000	2167	4500	9750	-99	-97	-95	-91
3	16-QAM	1/2	1333	2889	6000	13000	-96	-94	-91	-88
4	16-QAM	3/4	2000	4333	9000	19500	-93	-90	-88	-85
5	64-QAM	2/3	2667	5778	12000	26000	-89	-87	-84	-80
6	64-QAM	3/4	3000	6500	13500	29250	-88	-85	-83	-79
7	64-QAM	5/6	3333	7222	15000	32500	-87	-84	-81	-77
10	BPSK	1/2 x 2	167	N/A			-107	N/A		

5.5.2.2. Adjacent Channel Rejection

Adjacent channel rejection is measured by setting the requested signal's strength 3 dB above the rate dependent Sensitivity and raising the power of the interfering signal until 10% PER is caused for a PSDU length of 256 byte packets. The power difference between the interfering and requested channel is the corresponding adjacent channel rejection:

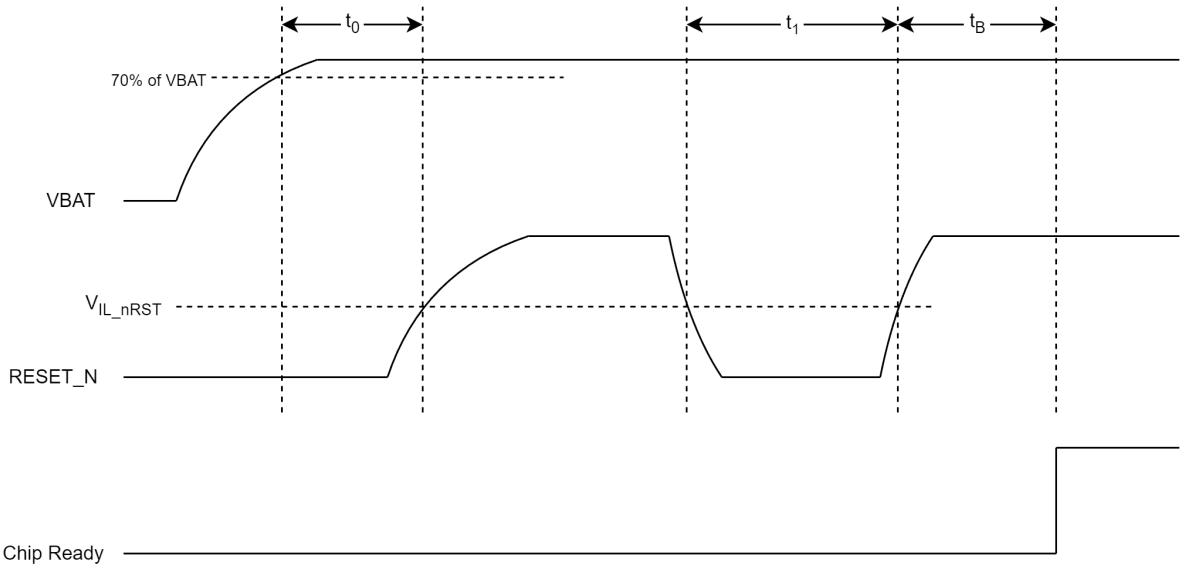
Bandwidth (MHz)	MCS Index	Modulation Scheme	Coding Rate	Adjacent Channel Rejection (dB) IEEE Spec	Adjacent Channel Rejection (dB)
4	0	BPSK	1/2	16	34
	2	QPSK	3/4	11	23
	4	16-QAM	3/4	4	21
	7	64-QAM	5/6	-2	3
8	0	BPSK	1/2	16	26
	2	QPSK	3/4	11	24
	4	16-QAM	3/4	4	23
	7	64-QAM	5/6	-2	10

5.5.3. Transmitter

Note: The following transmit power levels are for IEEE compliance for 802.11ah. This does not take into account any backoffs needed to adhere to regional spectrum compliance (eg, FCC, IC, TELEC).

Tx output power (1, 2 MHz BW)	Min (dBm)	Typical (dBm)	Max (dBm)
MCS 0	5.3	6.4	7.4
MCS 7	1.4	2.8	4.1

5.6. Digital Specifications

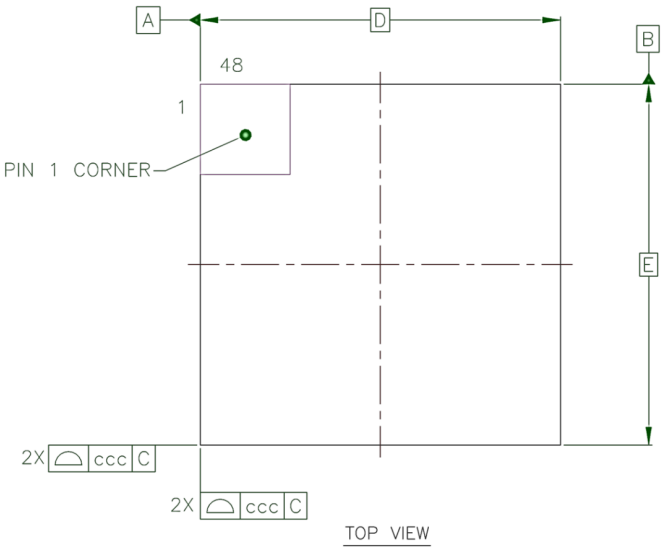


Parameters	Description	Min	Max	Unit
V_{IL_nRST}	Reset threshold	450		mV
t_0	Time between VBAT brought up (3.3V) and RESET_N being activated	50		µs
t_1	Duration of RESET_N signal level < VIL_nRST to reset the chip	1000		µs
t_B	Boot Time		6	ms

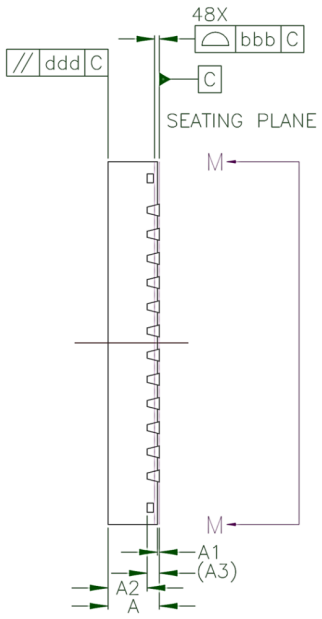
Parameters	Description	VDDIO	Min	Max	Unit
V_{IL_GPIO}	Low input threshold for all GPIO and SDIO pins	1.8	-0.3	0.63	V
		2.5	-0.3	0.7	V
		3.3	-0.3	0.8	V
V_{IH_GPIO}	High input threshold for all GPIO and SDIO pins	1.8	1.17	3.6	V
		2.5	1.7	3.6	V
		3.3	2.0	3.6	V
V_{OL_GPIO}	Low output voltage for all GPIO and SDIO pins assuming a 8mA load	1.8	0.13	0.38	V
		2.5	0.10	0.27	V
		3.3	0.08	0.18	V
V_{OH_GPIO}	High output voltage for all GPIO and SDIO pins assuming a 8mA load	1.8	1.34	1.70	V
		2.5	2.20	2.41	V
		3.3	3.07	3.23	V
V_{OL_SDIO}	Low output voltage for all SDIO pins assuming a 8mA load	1.8	0.17	0.52	V
		2.5	0.14	0.36	V
		3.3	0.11	0.24	V
V_{OH_SDIO}	High output voltage for all SDIO pins assuming a 8mA load	1.8	1.19	1.67	V
		2.5	2.10	2.39	V
		3.3	2.99	3.21	V

6. Package Information

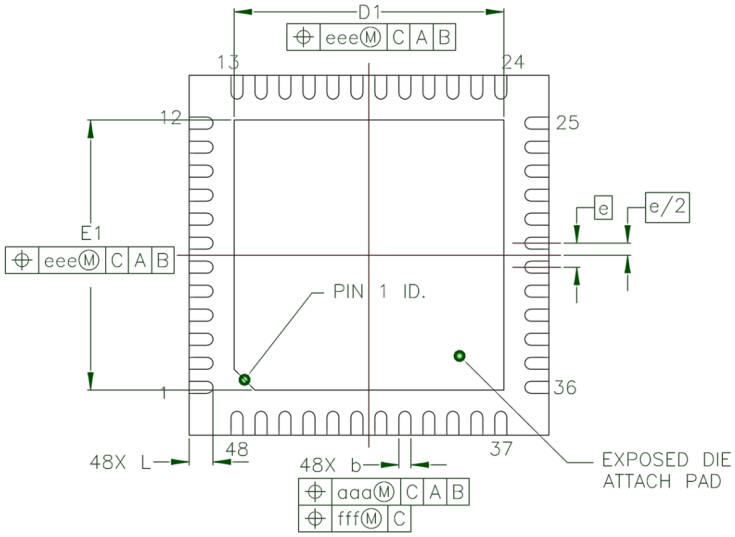
6.1. Package Dimensions



TOP VIEW



SIDE VIEW



BOTTOM VIEW
VIEW M–M

PACKAGE TYPE		QFN		
PIN COUNT		48		
DESCRIPTION	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
TOTAL THICKNESS	A	0.80	0.85	0.90
STAND OFF	A1	0	0.035	0.05
MOLD THICKNESS	A2	–	0.65	0.67
MATERIAL THICKNESS	A3	–	0.203 REF	–
PACKAGE SIZE	D	5.9	6	6.1
	E	5.9	6	6.1
EP SIZE	D1	4.4	4.5	4.6
	E1	4.4	4.5	4.6 (.01)
LEAD LENGTH	L	0.3	0.4	0.5
LEAD PITCH	e	0.4 BSC		
LEAD WIDTH	b	0.15	0.20	0.25
LEAD POSITION OFFSET	aaa	0.07		
LEAD COPLANARITY	bbb	0.08		
PACKAGE EDGE PROFILE	ccc	0.10		
MOLD FLATNESS	ddd	0.10		
EP POSITION OFFSET	eee	0.10		
	fff	0.05		

6.2. Thermal Properties

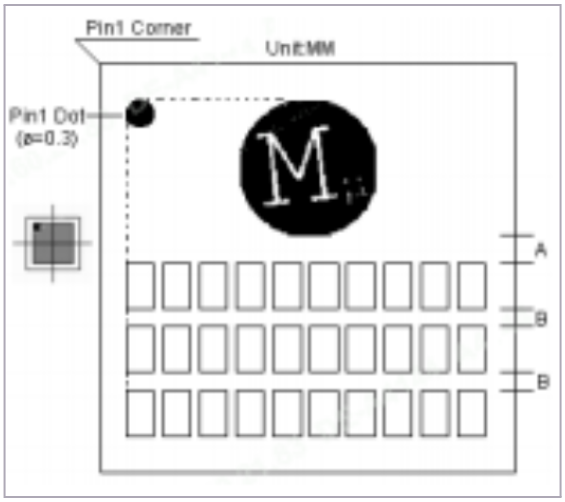
Pin number	PKG Size (mm)	Power (W)	Ta (°C)	Theta JA (°C/W)	Psi JT (°C/W)	Theta JC (deg C/W)
48	QFN 6x6	1	25	31.22	0.26	15.703

Ta: ambient Temperature, defined as the temperature of the surrounding environment expressed in °C. The temperature range can be found in the recommended operating conditions section of the datasheets.
Theta JA: thermal resistance junction-to-ambient
Psi JT: thermal characterization parameter between the junction and package top.
Theta TJ: junction temperature rise over case in deg C/ Watt of chip power dissipation.
Tj = junction temperature (during operation). It is determined by P x theta JA

*Power = power consumed by the device
**The maximum junction temperature should be controlled to </= 125 deg C
***The actual maximum junction temperature is determined using Theta JA, and depends on ambient temperature as well as power dissipation in the actual use.

JEDEC standards can be found at www.jedec.org under the JESD51 standard.

6.3. IC Markings

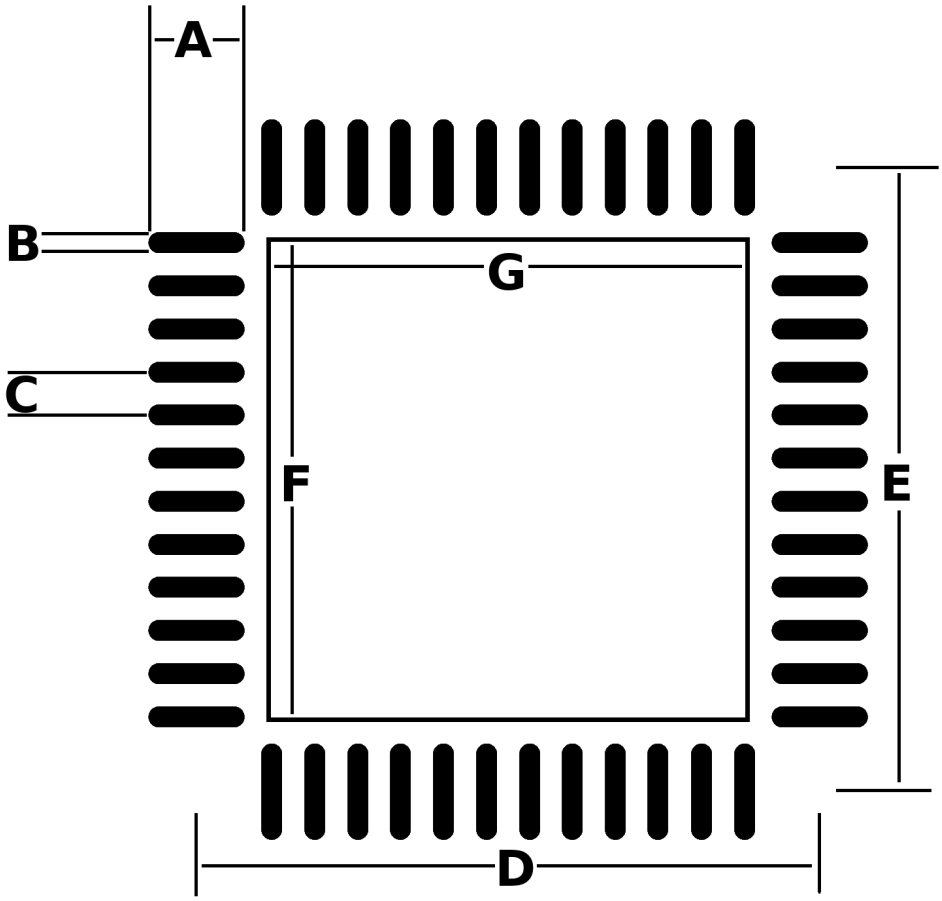


Line	Title	Example	Description
1	MMXXXXMDSn	MM6108MIQ	Device number; Optional: Custom Marketing Letter; Temperature Grade; Package Type;
2	TA12 YYWW	TA2103	Fab/Assembly codes; 2 digits for Silicon revision (Major, Minor - Internal Only); date code YYWW;
3	XXXXXXXX	MOR946N001	8 digits Assy Lot number;

* All Morse Micro ICs are lead-free

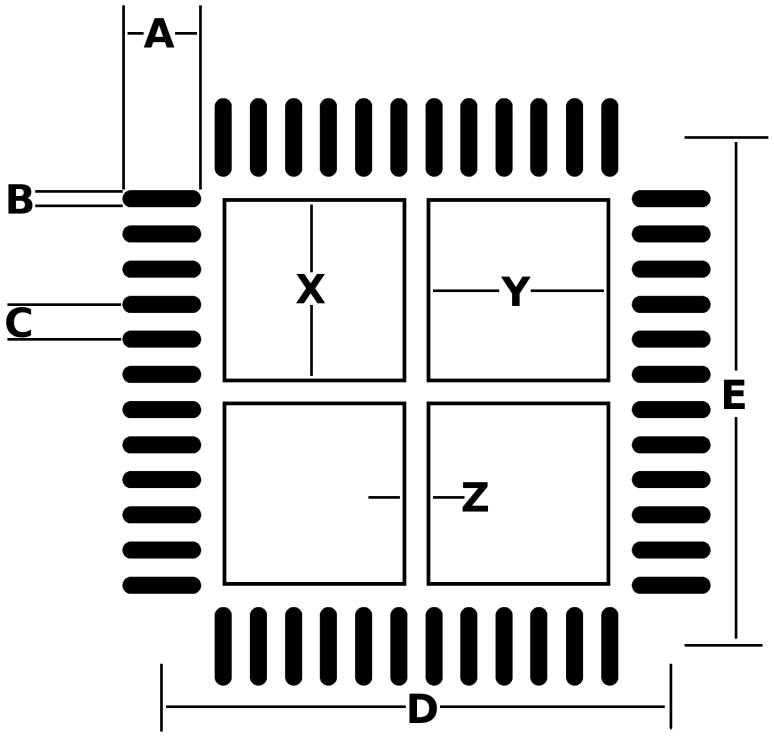
Legend	Title	Examples	Description
1	Major silicon Revision	0..9	Designated by a single number from 0 to 9
2	Minor silicon revision	0..9	Designated by a single number from 0 to 9
M	Custom Marketing suffix	M, L	M: 56 pin package (“Medium”) L: 64 pin package (“Large”)
D	Temperature Grade	I / C	I = -40℃ to 85℃; C = 0℃ to 70℃
S	Package Type code	Q / B	Q: QFN; B: FCBGA/BGA
n	Bond-Out Option	0..9	Designated by a single number 0..9

7. PCB Land Pattern



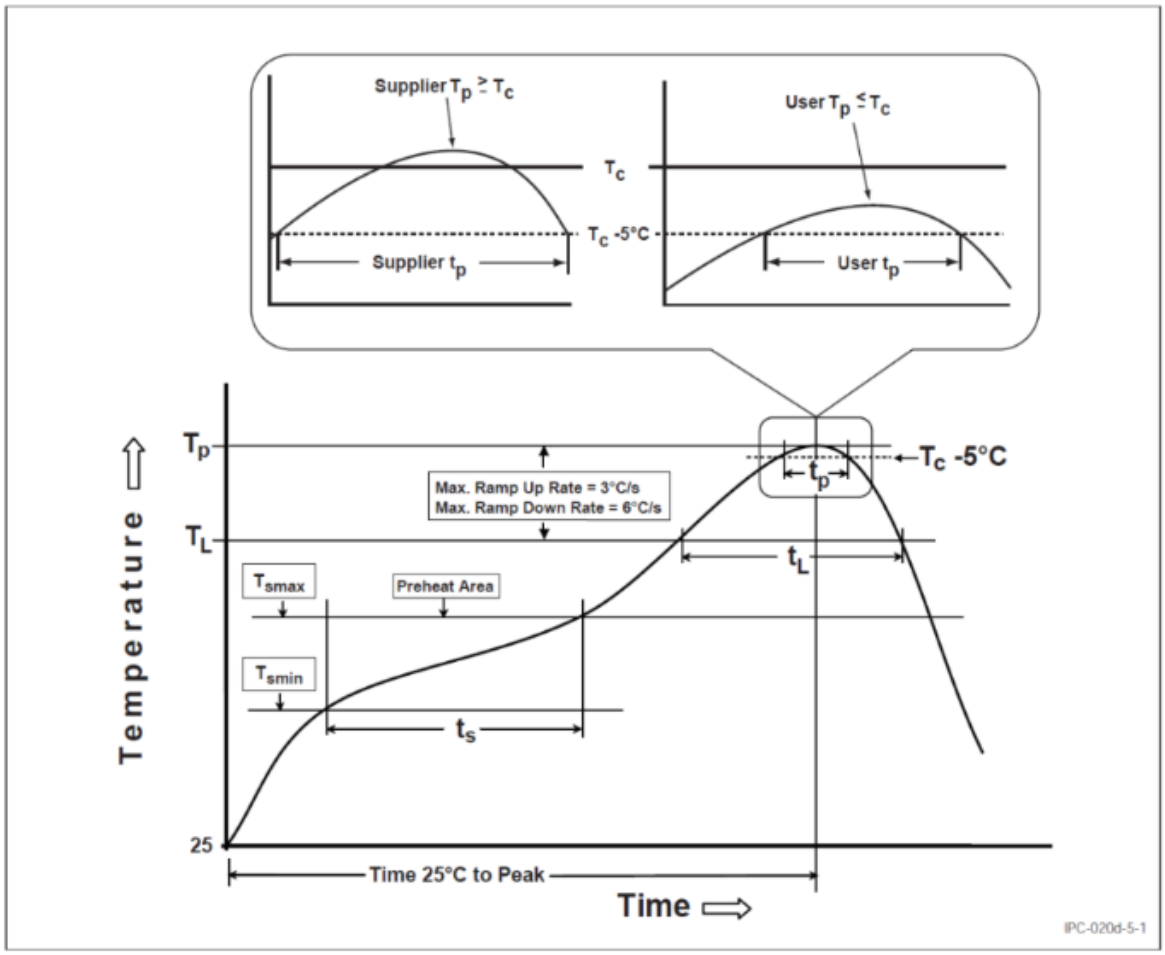
Key	Dimension (mm)
A	0.90
B	0.20
C	0.40
D	5.80
E	5.80
F	4.50
G	4.50

8. Solder Stencil Pattern



Key	Dimension (mm)
A	0.80
B	0.15
C	0.40
D	5.80
E	5.80
X	2.00
Y	2.00
Z	0.50

9. Recommended Soldering Profile



Pb-free (SAC Alloys) Process - Classification Temperature (TC)

Package Thickness	Volume mm3 < 350	Volume mm3 350 - 2000	Volume mm3 > 2000
< 1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
> 2.5 mm	250 °C	245 °C	245 °C

Profile Feature	Pb-free Assembly
Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	150 °C 200 °C 60-120 seconds
Ramp-up rate (TL to TP)	3 °C/second max.
Liquidus temperature (TL) Time (tL) maintained above TL	217 °C 60-150 seconds
Peak package body temperature (TP)	For users TP must not exceed the Classification temp in Table 4-2. For suppliers TP must equal or exceed the Classification temp in Table 4-2.
Time (tP)* within 5 °C of the specified classification temperature (TC), see Figure 5-1	30* seconds
Ramp-down rate (TP to TL)	6 °C/second max.
Time 25 °C to peak temperature	8 minutes max.
* Tolerance for peak profile temperature (TP) is defined as a supplier minimum and a user maximum	

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), TP shall be within +/- 2 °C of the live-bug TP and still meet the TC requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.

Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table 5-2.

For example, if TC is 260 °C and time tP is 30 seconds, this means the following for the supplier and the user.

For a supplier: The peak temperature must be at least 260 °C. The time above 255 °C must be at least 30 seconds.

For a user: The peak temperature must not exceed 260 °C. The time above 255 °C must not exceed 30 seconds.

Note 3: All components in the test load shall meet the classification profile requirements.

Note 4: SMD packages classified to a given moisture sensitivity level by using Producers or Criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification is desired.

10. Packaging and Labeling

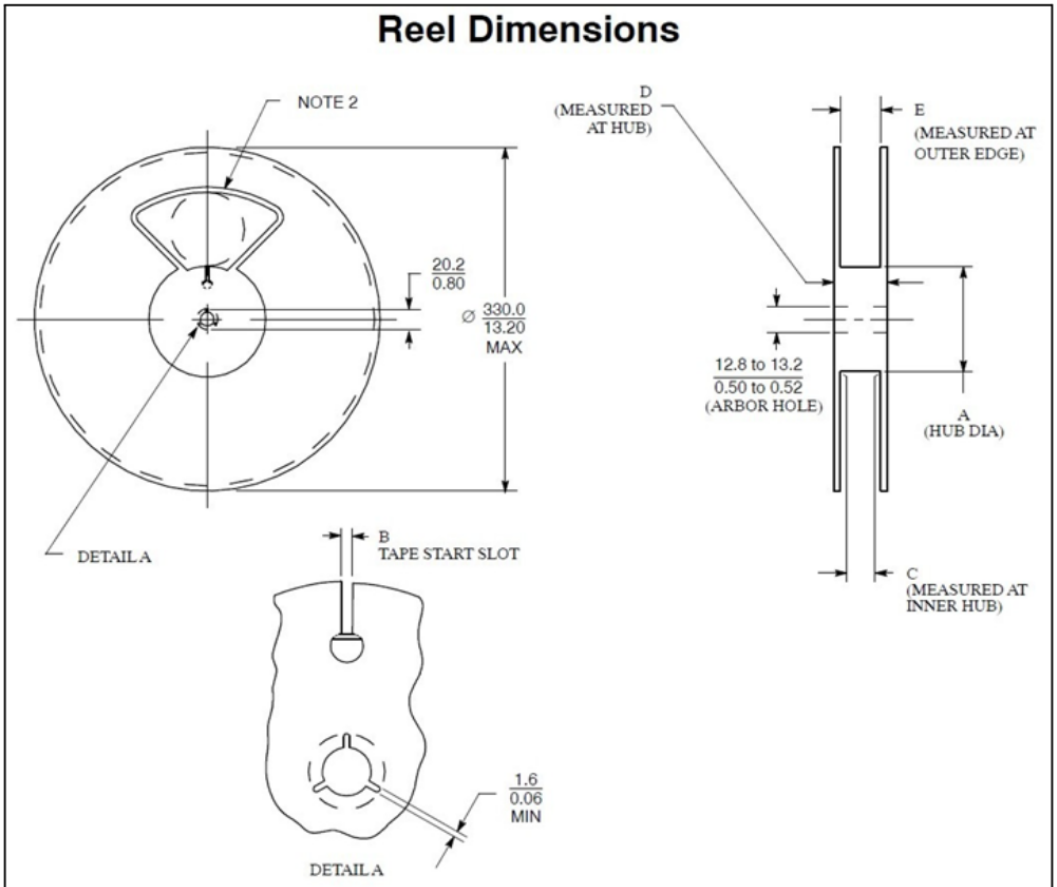
10.1. Tape & Reel Specification

Term	Definition
Product	MM6108
# Units	3,000
Reel Size	13 inches
Pizza Box	yes
Vacuum Seal	yes
Dry Bake	125 C / 24 hour (ML3)
Reel Pocket Dimensions	Refer to Figure 2
Pin 1 indicator	Marked on the chip

10.2. Tray Specification

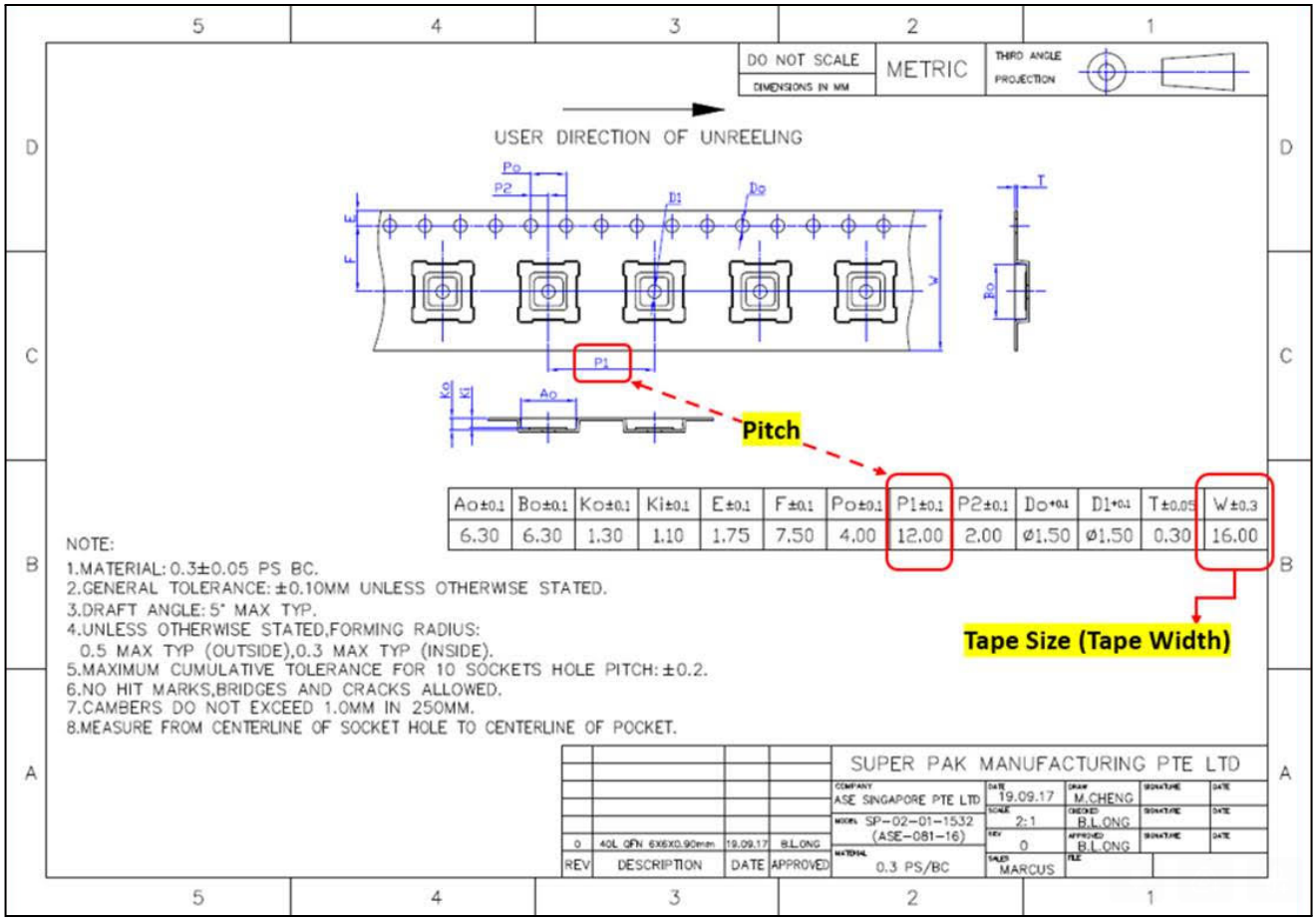
Term	Definition
Product	MM6108
# Units	490
Tray Size	322.6mm x 135.9mm
Pizza Box	No
Vacuum Seal	yes
Dry Bake	125 C / 24 hour (ML3)
Pin 1 indicator	Marked on the chip

10.3. Reel Dimensions



Reel Diameter	Tape Size	A mm (inches)		B mm (inches)		C mm (inches)		D (Max)	E (Max)
		Min	Max	Min	Max	Min	Max		
178.0 (7.01)	16.0 (0.63)		50.0 (1.97)	6.5 (0.26)	7.5 (0.30)	16.4 (0.65)	18.4 (0.72)	22.4 (0.88)	19.4 (0.76)
330.0 (12.99)	12.0 (0.47)	178.0 (7.01)		4.5 (0.18)	5.5 (0.22)	12.4 (0.49)	14.4 (0.57)	18.4 (0.72)	15.4 (0.61)
330.0 (12.99)	56.0 (2.20)	150.0 (5.91)		10.0 (0.39)	11.0 (0.43)	56.4 (2.22)	58.4 (2.30)	62.4 (2.46)	59.4 (2.34)
330.0 (12.99)	44.0 (1.73)	100.0 (3.94)		10.0 (0.39)	11.0 (0.43)	44.4 (1.75)	46.4 (1.83)	62.4 (2.46)	47.4 (1.87)
330.0 (12.99)	32.0 (1.26)	100.0 (3.94)		10.0 (0.39)	11.0 (0.43)	32.4 (1.28)	34.4 (1.35)	38.4 (1.51)	35.4 (1.39)
330.0 (12.99)	24.0 (0.94)	60.0 (2.36)		9.5 (0.37)	10.5 (0.41)	24.4 (0.96)	26.4 (1.04)	30.4 (1.51)	27.4 (1.08)
330.0 (12.99)	16.0 (0.63)			6.5 (0.26)	7.5 (0.30)	16.4 (0.65)	18.4 (0.72)	22.4 (0.88)	19.4 (0.76)
330.0 (12.99)	12.0 (0.47)			4.5 (0.18)	5.5 (0.22)	12.4 (0.49)	14.4 (0.57)	18.4 (0.72)	15.4 (0.61)
330.0 (12.99)	8.0 (0.31)	50.0 (1.97)		2.5 (0.10)	3.5 (0.14)	8.4 (0.33)	9.9 (0.39)	14.4 (0.57)	10.9 (0.43)
178.0 (7.01)	12.0 (0.47)	50.0 (1.97)		4.5 (0.18)	5.5 (0.22)	12.4 (0.49)	14.4 (0.57)	18.4 (0.72)	15.4 (0.61)
178.0 (7.00)	8.0 (0.31)	50.0 (1.97)		2.5 (0.10)	3.5 (0.14)	8.4 (0.33)	9.9 (0.39)	14.4 (0.47)	10.9 (0.43)
330.0 (12.99)	8.0 (0.31)	50.0 (1.97)		4.0 (0.16)	5.0 (0.20)	8.4 (0.33)	9.9 (0.39)	14.4 (0.57)	10.9 (0.43)
178.0 (7.00)	8.0 (0.31)	50.0 (1.97)		4.0 (0.16)	5.0 (0.20)	8.4 (0.33)	9.9 (0.39)	14.4 (0.57)	10.9 (0.43)

10.4. Tape and Device placement dimensions



Ao±0.1	Bo±0.1	Ko±0.1	Ki±0.1	E±0.1	F±0.1	Po±0.1	P1±0.1	P2±0.1	Do+0.1	D1+0.1	T±0.05	W±0.3
6.30	6.30	1.30	1.10	1.75	7.50	4.00	12.00	2.00	ø1.50	ø1.50	0.30	16.00

11. Handling and storage

The MM6108IQ IC is a moisture-sensitive device rated at Moisture Sensitive Level 3 (**MSL3**) per IPC/JEDEC J-STD-20.

After opening the moisture-sealed storage bag, modules that will be subjected to reflow solder or other high-temperature processes must be:

1. Mounted to a circuit board within 168 hours at factory conditions (≤30°C and <60% RH)

   OR

2. Continuously stored per IPC/JEDEC J-STD-033

IC's that have been exposed to moisture and environmental conditions exceeding packaging and storage conditions MUST be baked before mounting according to IPC/JEDEC J-STD-033. Failure to meet packaging and storage conditions will result in irreparable damage to modules during solder reflow.

12. Part Number and Ordering Information

Part Number	Packing Type	MOQ	Package	Description	Operating Ambient Temperature
MM6108CQ-T	Tray	490	QFN 6x6	IEEE 802.11ah Sub-1 GHz 1/2/4/8 MHz Wi-Fi HaLow SoC	-10°C to 70°C
MM6108CQ-TR	Tape & Reel	3000			
MM6108IQ-T	Tray	490	QFN 6x6	IEEE 802.11ah Sub-1 GHz 1/2/4/8 MHz Wi-Fi HaLow SoC	-40°C to 85°C
MM6108IQ-TR	Tape & Reel	3000			

13. Revision History

MM6108-ADS103-R; December 15th, 2023

- Add Power Sequencing requirements
- Add Vih, Vil, Voh and Vol specifications
- Add solder profile
- Add packaging
- Add chip markings
- Add sleep/wake pin sequencing

MM6108-ADS102-R; April 8th, 2022

- Updated table 5.5.1 RF Spectrum Range
- Added PCB land pattern and solder stencil
- Updated electrical characteristics
- Added Max/Min values

MM6108-ADS101-R; Nov. 4th, 2021

- Updated Recommended Operating conditions
- Updated Tx and Rx power consumption
- Updated Adjacent Current Rejection

MM6108-ADS100-R; June 1st, 2021

- Advance Data Sheet Initial release

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